IN THE CLAIMS:

1. (Currently Amended) In a multiprocessing computer system comprising a plurality of processing nodes interconnected through an interconnect structure, wherein the plurality of processing nodes includes a first processing node, a second processing node, and a third processing node, a method for lock request arbitration comprising:

~~the first processing node transmitting~~ receiving a lock request [[to]] at the second processing node from the first processing node;

~~the second processing node~~ determining, at the second processing node, whether the lock request is ready for service;

~~the second processing node~~ issuing a broadcast message from the second processing node to the first and the third processing nodes in response to determining that the lock request is ready for service;

~~the first processing node sending~~ receiving a first probe response [[to]] at the second processing node from the first processing node in response to sending the broadcast message; ~~and~~

~~the third processing node sending~~ receiving a second ~~probed~~ probe response [[to]] at the second processing node from the third processing node in response to sending the broadcast message;

in response to receiving the first and second probe response messages, granting lock ownership to the first processing node and transmitting from the second processing node to the first processing node a lock response message to inform the first processing node of the lock ownership.

2. (Original) The method as in claim 1, wherein determining whether the lock request is ready for service comprises:

the second processing node placing the lock request in a queue; and

the second processing node monitoring the queue to determine whether the lock request is ready for service.

3. (Original) The method as recited in claim 2, wherein monitoring the queue comprises: sequentially processing each preceding lock request in the queue.

4. (Original) The method as recited in claim 1, wherein the broadcast message informs the third processing node of servicing of the lock request.

5. (Original) The method as recited in claim 4, wherein the broadcast message includes a lock bit to inform the third processing node of the servicing of the lock request.

6. (Cancelled)

7. (Previously presented) The method as recited in claim 1, wherein the third processing node sends the second probe response when the third processing node ceases issuance of new requests.

8. (Cancelled)

9. (Cancelled)

10. (Currently Amended) In a multiprocessing computer system comprising a plurality of processing nodes interconnected through an interconnect structure, wherein the plurality of processing nodes includes a first processing node having ownership of a lock, a second processing node, and a third processing node, a method ~~whereby the first processing node releases~~ for releasing the ownership of the lock comprising:

~~the first processing node transmitting~~ receiving a lock release request [[to]] at the second processing node from the first processing node;

~~the second processing node~~ issuing a broadcast message from the second processing node to the first and the third processing nodes in response to receiving the lock release request; ~~and~~

~~each of the first and the third processing nodes sending~~ receiving, at the second processing node, a first corresponding probe response message from each of the first and the third processing nodes ~~to the second processing node~~ in response to sending the broadcast message;

in response to receiving the first corresponding probe response message from the first and the third processing nodes, transmitting a lock release message from the second processing node to the first processing node to release ownership of the lock.

11. (Original) The method as recited in claim 10, wherein the broadcast message informs the third processing node of completion of lock operations within the multiprocessing computer system.

12. (Original) The method as recited in claim 11, wherein the broadcast message includes a lock bit to inform the third processing node of the completion of the lock operations.

13. (Cancelled)

14. (Cancelled)

15. (Currently Amended) A multiprocessing computer system comprising:

a plurality of processing nodes interconnected through an interconnect structure to each other and to shared system resources, wherein the plurality of processing nodes comprises:

a first processing node configured to generate a lock request prior to commencing execution of an operation required access to the shared system resources;

a second processing node; and

a third processing node configured to receive and process the lock request, and transmit a first broadcast message to the first and the second processing nodes in response to determining that the lock request ~~to be~~ is ready for service;

wherein each of the first and the second processing nodes is configured to transmit

a corresponding first probe response message to the third processing node in response to receiving the first broadcast message;

wherein, in response to receiving the corresponding first probe response message from the first and the second processing nodes, the third processing node is configured to grant lock ownership to the first processing node and transmit lock response message to the first processing node to inform the first processing node of the lock ownership.

16. (Original) The multiprocessing computer system as recited in claim 15, wherein the third processing node comprises a queue for pending lock requests, wherein the third processing node is configured to place the lock request in the queue and to monitor the queue to determine when the lock request is ready for service.

17. (Original) The multiprocessing computer system as recited in claim 15, wherein the first broadcast message comprises:

a lock bit, wherein the third processing node is configured to set the lock bit in response to determining the lock request ready for service.

18. (Original) The multiprocessing computer system as recited in claim 15, wherein the interconnect structure includes a plurality of dual-unidirectional links.

19. (Original) The multiprocessing computer system as recited in claim 18, wherein each dual-unidirectional link in the plurality of dual-unidirectional links interconnects a respective pair of processing nodes from the plurality of processing nodes.

20. (Original) The multiprocessing computer system as recited in claim 18, wherein each dual-unidirectional link in the plurality of dual-unidirectional links performs packetized information transfer.

21. (Original) The multiprocessing computer system as recited in claim 15, wherein each of the plurality of processing nodes includes:

a plurality of circuit elements comprising:

a processor core,

a cache memory, and

a memory controller; and

a plurality of interface ports, wherein each of the plurality of circuit elements is coupled to at least one of the plurality of interface ports.

22. (Original) The multiprocessing computer system as recited in claim 21, wherein the plurality of circuit elements further includes:

a bus bridge;

a graphics logic;

a bus controller; and

a peripheral device controller.

23. (Original) The multiprocessing computer system as recited in claim 21, wherein at least one of the plurality of interface ports in the each of the plurality of processing nodes is connected to a corresponding one of the plurality of dual-unidirectional links.

24. (Original) The multiprocessing computer system as recited in claim 15, further comprising:

a plurality of system memories; and

a plurality of memory buses, wherein each of the plurality of system memories is coupled to a corresponding one of the plurality of processing nodes through a respective one of the plurality of system buses.

25. (Cancelled)

26. (Cancelled)

27. (Previously presented) The multiprocessing computer system as recited in claim 15, wherein the second processing node is further configured to cease issuance of new requests and to transmit the corresponding first probe response message upon the cessation of the issuance.

28. (Cancelled)

29. (Currently amended) The multiprocessing computer system as recited in claim [[28]]15, wherein the first processing node is configured to commence the execution of the lock operation after receiving the ~~second target done~~ lock response message, and wherein the first processing node is further configured to transmit a lock release request to the third processing node after completion of the execution of the lock operation.

30. (Original) The multiprocessing computer system as recited in claim 29, wherein the third processing node is configured to transmit a second broadcast message to the first and the second processing nodes in response to receiving the lock release request.

31. (Original) The multiprocessing computer system as recited in claim 30, wherein each of the first and the second processing nodes is configured to transmit a corresponding second probe response message to the third processing node in response to the second broadcast message.

32. (Currently amended) The multiprocessing computer system as recited in claim 31, wherein the third processing node is configured to transmit a second ~~target done~~ lock response message to the first processing node in response to receiving the corresponding second probe response messages from the first and the second processing nodes.

33. (Currently amended) The multiprocessing computer system as recited in claim 32, wherein the third processing node is configured to place a pending lock request into service upon transmission of the second ~~target done~~ lock response message, and the pending lock request is

generated by one of the plurality of processing nodes and is stored within the third processing node.